IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Stephen R. Fox, et al.

Serial No: 09/884,670

Filed: June 19, 2001

For: DIVOT REDUCTION IN SIMOX LAYERS

Examiner: Ron E. Pompey

Art Unit: 2814

Docket: YOR920010104US1 (14270)

Dated: August 25, 2003

Commissioner for Patents
United States Patent and Trademark Office
Alexandria, VA 22313-1450

DECLARATION OF DEVENDRA K. SADANA UNDER 37 C.F.R. §1.132

Sir:

I, Devendra K. Sadana, hereby declare and say that:

(1) I am one of the applicants named in U.S. Application Serial No. 09/884,670, filed with the United States Patent and Trademark Office on June 19, 2001;

(2) The present invention is directed to a method for reducing the formation of divot and tile defects at the superfacial Si-containing layer of an SOI substrate.

(3) I am familiar with the subject matter disclosed in U.S. Application Serial No. 09/884,670, filed June 19, 2001; and have reviewed the applied references, namely U.S. Patent No. 6,090,689 to Sadana, et al ("Sadana '689"), U.S. Patent No. 5,534,446 to Tachimori, et al. ("Tachimori, et al.") and U.S. Patent No. 5,930,643 to Sadana, et al. ("Sadana '643") that was cited in the Office Action dated March 26, 2003;

(4) Additional experiments and data have been carried out to establish that the claimed annealing ambient is not obvious relative to the disclosures of Sadana '643, Sadana '689, and Tachimori, et al. cited by the Examiner in the Office Action dated March 26, 2003;

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(5) The experiments performed and reported in this Declaration were conducted under my direction;

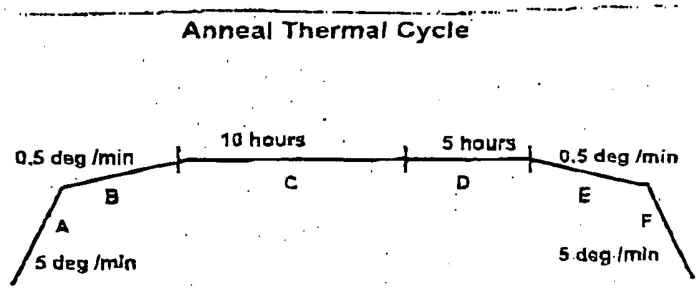
(6) Experiments have been performed to show unexpected results, in terms of reduced divot and tile formation at the Si surface of a silicon-on-insulator substrate, that can be obtained using an annealing ambient which falls within the scope of Claim 1 of the '670 application. More specifically, it was unexpectedly determined that the use of an ambient gas comprising 0 to about 90% oxygen and from about 10 to about 100% of N_2 is capable of providing an SOI substrate that contains a superfacial Si-containing layer that has a substantial reduced number of tile or divot defects, as compared to SOI substrates that are not annealed in the claimed gas ambient. The reduction of divot formation due to the inventive method recited in the present application was unexpected because the claimed annealing atmosphere was considered by those having ordinary skill in the art to effect only buried oxide formation. A comparative experiment was also conducted using the annealing ambient disclosed in Tachimori, et al., where the reduction in tiles and surface divots in the SOI layer is not produced using an oxidizing ambient that includes a mixture of oxygen and Ar.

(7) **EXPERIMENTAL PROTOCAL**

Si substrates were first provided for experimentation of the annealing process disclosed within the scope of Claim 1 of the '670 application and the annealing process disclosed in Tachimori, et al. using the same SOI substrate processing steps. More specifically, a Si substrate was provided and then implanted with a ½ base implant conducted

with a dosage of approximately 1.6×10^{17} atoms/cm^2 of O+ ions at an energy of approximately 212 keV, and at a temperature of approximately 365°C. Following cooling of the substrate to room temperature, a cleaning process was conducted comprising a diluted HF chemical clean comprising 10 parts deionized water to 1 part HF, where the HF concentration is approximately 49%; a brush clean; and 2 part standard clean including a first solution of hydrogen peroxide, ammonium hydroxide, and water followed by a second solution of hydrogen peroxide, hydrochloric acid and water. The substrate was then implanted a second time with a ½ base implant conducted with a dosage of approximately 1.6×10^{17} atoms/cm^2 of O+ ions at an energy of approximately 212 keV, and a temperature of approximately 365°C. Following cooling, the substrate was cleaned with a diluted HF chemical clean composed of 10 parts deionized water to 1 part HF, where the HF concentration is approximately 49%; followed by a brush clean; and subsequent 2 part standard chemical clean including a first solution of hydrogen peroxide, ammonium hydroxide, and water followed by a second solution of hydrogen peroxide, hydrochloric acid and water. The substrate was then subjected to a nominal room temperature implant with a dosage of approximately 2.0×10^{15} atoms/cm^2 of O+ ions at an energy of approximately 212 keV and thereafter subsequently cleaned using a diluted HF chemical clean composed of 10 parts deionized water to 1 part HF, where the HF concentration is approximately 49%, followed by a 2 part standard chemical clean process including a first solution of hydrogen peroxide, ammonium hydroxide, and water followed by a second solution of hydrogen peroxide, hydrochloric acid and water.

The above described SOI substrates were then subjected to the following annealing thermal cycle, where the reference letters correspond to the annealing conditions described below:



SOI substrates annealed in accordance with the procedures disclosed in the '670 patent used the following annealing ambient and temperature ranges in the above thermal cycle:

A = Temperature ramped from 600° – 1000°C at 5 deg/min in N_2 + 5% O_2 ambient.

A = Temperature ramped from 1000° – 1150°C at 5 deg/min in N_2 + 4% O_2 + 1.45E-4 % Trichloroethylene ambient.

B = Temperature ramped from 1150 °– 1320°C at 0.5 deg/min in N_2 + 4% O_2 – 1.45E-4 % Trichloroethylene ambient.

C = Temperature constant 1320°C for 10 hrs in N_2 + 45% O_2 + 1.45E-4 % Trichloroethylene ambient.

D = Temperature constant 1320°C for 5 hrs in N_2 + 4% O_2 + 1.45E-4 % Trichloroethylene ambient.

E = 1320° – 1150°C cool down in N_2 + 4% O_2 + 1.45E-4 % Trichloroethylene ambient.

F = 1150° – 600°C cool down in N_2 ambient.

SOI substrates prepared in comparative annealing ambient, similar to the annealing ambient disclosed in Tachimori, et al. used the following annealing ambient and temperature ranges in the above thermal cycle:

A = Temperature ramped from 600° – 1000°C at 5 deg/min in Ar + 5% O_2 ambient.

A = Temperature ramped from 1000° – 1150°C at 5 deg/min in Ar + 4% O_2 + 1.45E-4 % Trichloroethylene ambient.

B = Temperature ramped from 1150° – 1320°C at 0.5 deg/min in Ar + 4% O_2 + 1.45E-4 % Trichloroethylene ambient.

C = Temperature constant at 1320°C for 10 hrs in Ar + 45% O_2 + 1.45E-4 % Trichloroethylene ambient.

D = Temperature constant at 1320°C for 5 hrs in an Ar + 4% O_2 + 1.45E-4 % Trichloroethylene ambient.

E = 1320° – 1150°C cool down in Ar + 4% O_2 + 1.45E-4 % Trichloroethylene ambient

F = 1150° – 600°C cool down in N_2 ambient.

(8) **EXPERMENTAL RESULTS**:

The results of the above described experiments are shown in micrographs, taken on a KLA 2139 optical process yield wafer inspection system. FIG. 1 depicts a micrograph of an SOI substrate processed in an annealing ambient similar to that disclosed in Tachimori, et al., where the annealing ambient gas of the Tachimori, et al. reference comprises N_2, Ar and O_2. FIG. 1 clearly depicts the formation of tile/divot defects in the superfacial Si layer of the SOI substrate. Each shadow region on the superficial Si layer represents a divot/tile defect, where reference number 10 depicts a deep divot having a crystalline structure. Therefore, the annealing ambient disclosed in Tachimori, et al. fails to produce an SOI substrate having a superfacial Si layer having a substantially divot or tile free surface.

FIG. 2 depicts a micrograph of an SOI substrate processed in an annealing ambient within the scope of the claimed annealing process disclosed in the '689 application. The superfacial Si layer formed in the inventive annealing ambient produces a mottled Si surface without the shadowing that is representative of a surface having tile/divot defect crystalline

structure. It is noted that the dark region positioned at the center of FIG. 2 is an artifact, i.e. dirt, on the sample surface and is not a divot or tile defect. Therefore, FIG. 2 clearly depicts a superfacial Si layer substantially free of tile or divot defects.

These particular results, i.e., the reduction of tile or divot defects at the superfacial Si layer of an SOI substrate, are unexpected and are not obvious from the disclosure of Tachimori,. et al., since Tachimori, et al. do not produce a substantially divot or tile free superfacial Si layer or recognize the effect of an annealing ambient annealing gas disclosed in the '689 application.

(9) All statements made herein, of my own knowledge, are true, and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made may be punishable by fine or imprisonment or both, under Section 1001 Title 18 of the U.S. code and that such willful false statements may jeopardize the validity of the application or any patent issuing therefrom.

Dated: August 26, 2003

Devendra Sadana
Devendra Sadana